REMARKS

Claims 1-12 are pending in this application of which claims 1, 6, 7, and 8 are independent.

Claims 1-12 have been newly rejected, as follows:

1. Claims 1-6 and 8-12 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Nagata et al., "Measurements and Analysis of Substrate Noise Waveform in Mixed Signal IC Environment" (hereinafter "Nagata Measurements"), in view of Nagata et al., "Physical Design Guides for Substrate Noise Reduction in CMOS Digital Circuits" (hereinafter "Nagata CMOS"); and

2. Claim 7 has been rejected under 35 U.S.C. §103(a) as being unpatenable over Nagata Measurements in view of Nagata CMOS and further in view of Mitra et al., "Substrate-Aware Mixed Signal Macrocell Placement in WRIGHT."

The rejections are respectfully traversed.

Newly-cited prior art, Nagata CMOS, was authored in part by the inventors of this application, and was published (March 2001) within one year of the U.S. filing date (October 17, 2001) and after the filing date (February 2, 2001) of the Japanese patent application from which priority has been claimed. Normally, Nagata CMOS would not constitute prior art on which a claim rejection could be based. However, the Information Disclosure Statement filed concurrently with this application cites Nagata CMOS as part of an IEEE conference of May 2000 during which this technology was allegedly discussed. It is noted that this citation was taken from taken from a European Search Report for the European counterpart application (EP 2001126335). The citations in both the European Search Report and the Information Disclosure Statement are incorrect. However, it is based on these citations which the Examiner assumes

that Nagata CMOS constitutes prior art. Applicants submit that in view of the following, Nagata CMOS is not prior art to the present application.

Enclosed herein are Rule 1.132 inventor declarations regarding the IEEE Conference. (***See Encls. 1 & 2***). Also, an Information Disclosure Statement filed concurrently herewith correctly cites Nagata CMOS, cites the Table of Contents for Proceedings of the IEEE 2000 Custom Integrated Circuits Conference (hereinafter "IEEE Conference") to which the Examiner has referred, and cites an article entitled "Quantitative Characterization of Substrate Noise for Physical Design Guides in Digital Circuits" (hereinafter "Nagata Quantitative Characterization")

In their declarations, inventors Mr. Nagata and Mr. Iwata state that they are familiar with the prosecution of this application and understand that the Examiner rejects the claims citing at least Nagata CMOS as prior art. (***See Encls. 1 & 2,*** ¶**2**). Moreover, the inventors state that they understand that the Examiner cited Nagata CMOS to identify the subject matter which was disclosed at the Proceedings of the IEEE 2000 Custom Integrated Circuits Conference, held in Florida, U.S., in May of 2000 (hereinafter the "IEEE Conference"). (***See Encls. 1 & 2,*** ¶**2**). It is further the inventors understanding that the subject matter on which the Examiner relies corresponds to the claimed subject matter relating to representing a digital circuit and generating an analysis model in accordance with a time-division group of parasitic capacitors. (***See Encls. 1 & 2,*** ¶**2**).

Inventors Nagata and Iwata have knowledge of the subject matter disclosed at the IEEE conference. (***See Encls. 1 & 2,*** ¶**3**). More particularly, the Table of Contents for the "Proceedings of the IEEE 2000 Custom Integrated Circuits Conference" and accompanying article entitled, "Quantitative Characterization of Substrate Noise for Physical Design Guides in

Digital Circuits"[1] (hereinafter "Nagata Quantitative Characterization), which are submitted in the IDS filed concurrently herewith, identify the subject matter that was disclosed at the IEEE conference. (***See Encls. 1 & 2,*** **¶4**). Contrary to the Examiner's assumption, Nagata CMOS was NOT disclosed or disseminated in any manner during the IEEE Conference. (***See Encls. 1 & 2,*** **¶3**). Rather, the Nagata CMOS article was published in March 2001, within one year of the U.S. filing date. (***See Encls. 1 & 2,*** **¶3**).

Evidence submitted with the IDS corroborates the statements made by the inventors. For example, section 5-7 of the Table of Contents lists Nagata Quantitative Characterization as being disclosed in the IEEE conference. Also, Nagata Quantitative Characterization is identified as being published in IEEE 2000 Custom Integrated Circuits Conference, and the page numbers correspond to those listed in section 5-7 of the Table of Contents. On the other hand, nowhere does the Table of Contents disclose Nagata CMOS as part of the IEEE Conference. The page numbers 539 – 549 of this article do not even correspond to the page numbers of the Table of Contents, nor does the publication information ("IEEE Journal of Solid0State Circuits, Vol. 36, No. 3, March 2001") have any correlation to the IEEE Conference.

Also, Nagata CMOS does NOT constitute 102(a) prior art because while the Nagata CMOS has a publication date between the Japanese counterpart application filing date and the effective filing date of the present application, Nagata CMOS was authored by the inventors of the present application. In other words, Nagata CMOS is applicant's own work, and therefore cannot be used as 102(a) prior art.

Submitted concurrently herewith are declarations by the inventors who are also co-authors of Nagata CMOS. (***See Encls. 3-4***). In these declarations, the Mr. Nagata and Mr.

[1] Mr. Nagata and Mr. Iwata, the inventors of the '994 application, co-authored the Nagata Quantitative Characterization article with three others.

Iwata, inventors of the present application, declare that they invented the subject matter covered by the claims of the present application. (***See Encls. 3 & 4,*** **¶2**). While the inventors co-authored the Nagata CMOS article, they state that the other co-authors did not invent the subject matter claimed in the present application. (***See Encls. 3 & 4,*** **¶¶3-4**). Moreover, the other co-authors (Takashi Morie, Katsumasa Hijikata and Jin Nagai) were working under the direction of Mr. Nagata and Mr. Iwata when co-authoring the subject matter claimed in this application. Accordingly, Nagata CMOS is applicant's own work, and therefore cannot be used as 102(a) prior art.

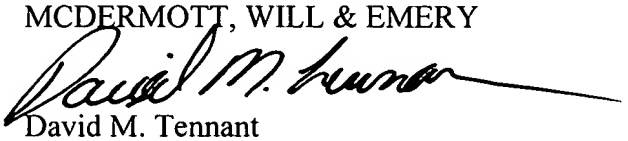
Also submitted concurrently herewith is an English translation Japanese Patent Application No. 2001-026795, filed February 2, 2001, and a certificate of translation, so as to preemptively remove any references as prior art that have a publication date between February 2, 2001 and the filing date of the present application.

In accordance with the foregoing, Nagata CMOS does not constitute prior art as of the date of the IEEE conference. The rejections citing claims 1-12 are no longer valid. Withdrawal of these rejections is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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Enclosures:

1. Declaration of Makoto Nagata, #1
2. Declaration of Atsushi Iwata, #1
3. Declaration of Makoto Nagata, #2
4. Declaration of Atsushi Iwata, #2
5. English Translation of Japanese Priority Application and Certificate of Translation

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